## Chapter 1. CoreSight SoC

### Overview

CoreSight SoC is a solution for debug and trace of complex SoCs. We can access system AXI, AHB and APB via JTAG interface. In Sirius, CoreSight SoC includes 5 trace soruces, one ETM in cortex-M7 and quad ETMs in cortex-A7 MPcore.

### 1.2 Block Diagram



Fig. 1.1 CoreSight SoC block diagram

### 1.3 Features

* Access to debug features and on-chip AXI, AHB, APB buses through a JTAG or Serial Wire Debug(SWD) interface
* 16KB on-chip sram ETB embedded in CoreSight SoC
* Trace source includes one M7 ETM, quad A7 ETMs
* Support up to 8-bit trace data output
* Support up to 150MHz trace clock output
* Support one M7 and quad A7 trace simultaneously
* 64-bit timestamp embedded in CoreSight SoC